What is claimed is:

1. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, the substrate having been provided with a patterned and etched layer of gate oxide over the surface there-of and a patterned and etched layer of gate material over said patterned gate oxide, a LDD impurity implant into the substrate having been performed and annealed self-aligned with the patterned and etched layer of gate material;

performing a plasma treatment of the patterned and etched layer of gate material and exposed surfaces of the substrate; and

creating spacers over sidewalls of the patterned and etched layer of gate material.

2. The method of claim 1, the plasma exposure being a H_2 based plasma exposure.

3. The method of claim 1, the plasma exposure being an O_2 based plasma exposure.

4. The method of claim 1, the plasma exposure being a N_2 based plasma exposure.

5. The method of claim 1, additionally pocket implants having been performed into the substrate after the LDD impurity implants have been performed.

6. The method of claim 1, additionally completing the gate electrode and conductive interconnects there-to after creating spacers over sidewalls of the patterned and etched layer of gate material.

7. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing an impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing a plasma treatment of the sidewalls of the gate electrode and the exposed substrate;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

8. The method of claim 7, the plasma treatment being a H_2 based plasma exposure.

9. The method of claim 7, the plasma treatment being an O_2 based plasma exposure.

10. The method of claim 7, the plasma treatment being a N_2 based plasma exposure.

11. The method of claim 7, the impurity implant comprising LDD implants.

12. The method of claim 7, the impurity implant comprising LDD implants followed by pocket implants.

13. The method of claim 7, the impurity implant being followed by an anneal.

14. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing a H_2 based plasma treatment of the sidewalls of the gate electrode and the exposed substrate;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

15. The method of claim 14, the impurity implants comprising LDD implants.

16. The method of claim 14, the impurity implants comprising LDD implants followed by pocket implants.

17. The method of claim 14, the impurity implants being followed by an anneal.

18. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing an O_2 based plasma treatment of the sidewalls of the gate electrode and the exposed substrate;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

19. The method of claim 18, the impurity implants comprising LDD implants.

20. The method of claim 18, the impurity implants comprising LDD implants followed by pocket implants.

21. The method of claim 18, the impurity implants being followed by an anneal.

22. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing impurity implants into the exposed substrate, self-aligned with the gate electrode;

performing a N_2 based plasma treatment of the sidewalls of the gate electrode and the exposed substrate;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

23. The method of claim 22, the impurity implants comprising LDD implants.

24. The method of claim 22, the impurity implants comprising LDD implants followed by pocket implants.

25. The method of claim 22, the impurity implants being followed by an anneal.

26. A method of manufacturing a gate electrode of improved channel effect and improved gate oxide reliability, comprising:

providing a substrate, an active surface having been bounded over the substrate by creating regions of field isolation;

creating a layer of gate oxide over the active surface;

creating a layer of gate material over the gate oxide;

patterning and etching the layer of gate material and layer of the gate oxide, creating a gate electrode having sidewalls over the active surface, exposing the substrate;

performing a LDD impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing a pocket impurity implant into the exposed substrate, self-aligned with the gate electrode;

performing an anneal of the LDD and pocket impurity implants;

performing a H_2 based or an N_2 based or an O_2 based plasma treatment of the sidewalls of the gate electrode and the exposed substrate;

creating spacers over the sidewalls of the gate electrode; and

completing the gate electrode, including conductive interconnects there-to.

27. A method of manufacturing a gate electrode, comprising:

providing a substrate;

forming a patterned gate oxide over said substrate;

forming a patterned gate material over said patterned gate oxide;

forming a pair of LDD structures in said substrate and respectively adjacent to said patterned gate oxide;

performing a plasma treatment to said patterned gate material and said substrate; and

respectively forming a pair of spacers over sidewalls of said patterned gate oxide and gate material.

28. The method of claim 27, the plasma treatment being a H_2 based plasma treatment.

29. The method of claim 27, the plasma treatment being an O_2 based plasma treatment.

30. The method of claim 27, the plasma treatment being a N_2 based plasma treatment.

31. The method of claim 27, the forming a pair of LDD structures being followed by an anneal.